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10/619,816	07/14/2003	Mark C. Johnson	SJO920030041US1	7645

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EXAMINER	
TRUONG, LOAN	
ART UNIT	PAPER NUMBER
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/619,816	JOHNSON ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-11,13-16,18-22,24-27 and 29-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-6, 8-11, 13-16, 18-22, 24-27, 29-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Request for Continued Examination on December 21, 2006 in application 10/619,816.

2. Claims 1, 3-6, 8-11, 13-16, 18-22, 24-27, 29-36 are presented for examination with claims 2, 7, 12, 17, 23 and 28 are cancel. Claims 1, 6, 11, 16, 22 and 27 are amended.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 3-6, 8-11, 13-16, 18-22, 24-27 and 29-36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 3-4, 6, 8-11, 13-16, 18-20, 22, 24-27 and 29-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson (US 6,345,349) in further view of Wang et al. (US

2004/0117606) in further view of Rahman et al. (US 5,590,337) in further view of Sharma et al. (US 7,047,475).

In regard to claim 1, Coulson disclosed an apparatus for managing errors in prefetched data, the apparatus comprising:

a prefetch module configured to prefetch a data packet from a first location (*main memory, fig. 2, 202-1, col. 6 lines 41-51)* into a second location (*sector buffer, fig. 3, 213, col. 6 lines 41-51);*

a validation module configured to determine that the prefetched data packet contains an uncorrectable error (*ECC correction circuitry, fig. 2, 207, col. 3 lines 1-4)*;

a transfer module configured to transfer the prefetched data packet from the second location (*memory interface, fig. 2, 203, col. 3 lines 24-31)* if the request is received (*from the sector buffer the requested data is then transferred to the processor via bus, fig. 3, 213, 204, col. 6 lines 41-51)*; and

an error recovery module configured to selectively initiate an error recovery process for the transferred prefetched data packet that has been determined to contain an uncorrectable error (*ECC correction circuitry, fig. 2, 207, col. 3 lines 24-31).*

Coulson does not explicitly teach the apparatus for managing errors in prefetched data by aniticipation of receiving a request for the prefetched data packet prior to receiving the request.

Wang et al. teach the method and apparatus for dynamically conditioning statically produced load speculation and prefetches using runtime information by

implementing a table for each prefetch instruction within programs wherein column 606 represents a usage prediction as to whether the data to be prefetched as a result of executing a prefetch instruction will be used or not *(paragraph 0028)*.

It would have been obvious to modify the apparatus of Coulson by adding Wang et al. apparatus for dynamically conditioning statically produced load speculation and prefetches using runtime information. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would optimize computational throughput *(paragraph 0004)*.

Coulson and Wang et al. does not explicitly teach the apparatus for an identification module configured to associate an identifier with the prefetched data packet prior to receiving the request if prefetched data packet contains the uncorrectable error.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag *(fig. 4, 308)* wherein indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error *(col. 9 lines 15-18)*.

It would have been obvious to modify the apparatus of Coulson and Wang et al. by adding Rahman et al. uncorrectable memory error flag. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide faster interaction with the microprocessor *(col. 1 lines 24-27)* and increase the speed at which data can be accepted from, and provided to, the microprocessor *(col. 1 lines 46-48)*.

Coulson, Wang et al. and Rahman et al. does not explicitly teach the identifier being stored in the second location with the data packet.

Sharma et al. teach of a CRC encoding scheme for conveying status information by implementing a sending node buffer comprising of an error status bit (*fig. 5, 228, col. 7 lines 24-43).*

It would have been obvious to modify the apparatus of Coulson, Wang et al. and Rahman et al. by adding Sharma et al. CRC encoding scheme for conveying status information. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would improve detection and/or correction of link errors occurring during transmission (*col. 2 lines 6-8).*

In regard to claim 3, Coulson disclosed the apparatus of claim 1, wherein the identifier is stored in the second location with the prefetched data packet (*command block is constructed in command structure cache and stored in main memory to be transfer to sector buffer on a read/write operation, fig. 2, 221, 202-1, 213, col. 7 lines 10-22 and col. 6 lines 41-51 and lines 62-66).*

In regard to claim 4, Coulson disclosed the apparatus of claim 1, wherein the validation module is further configured to store an address for the prefetched data packet within the first location (*command block stored in main memory contains an address in mass storage portion and address in main memory portion, fig. 2, 202-1, 202-2, col. 7 lines 14-22).*

In regard to claim 6, Coulson disclosed an apparatus for managing errors in prefetched data, the apparatus comprising:

a request module configured to request a transfer of a data packet from a first location (*main memory, fig. 2, 202-1, col. 6 lines 41-51)* by way of a communication bus (*processor received data transfer from mass storage device via bus, fig. 2, 201, 202, 204, col. 3 lines 25-31)*;

a data transfer interface configured to prefetch the data packet from the first location (*main memory, fig. 2, 202-1, col. 6 lines 41-51)* into a second location (*memory interface, fig. 2, 203, col. 3 lines 24-31)* prior to receiving the request and transferring the data to the request module across the communication bus (*data bus, fig. 3, 204, col. 3 lines 39-42)*, the data transfer interface further configured to determine that the prefetched data packet contains an uncorrectable error (*ECC correction circuitry, fig. 2, 207, col. 3 lines 1-4)*, and to selectively initiate an error recovery process for the prefetched data packet if the prefetched data packet is transferred to the request module (*data is transfer into sector buffer after the error correction code is used to check and correct data if necessary, fig. 3, 213, col. 6 lines 41-51.*

Coulson does not explicitly teach the apparatus for managing errors in prefetched data by aniticipation of receiving a request for the prefetched data packet prior to receiving the request.

Wang et al. teach the method and apparatus for dynamically conditioning statically produced load speculation and prefetches using runtime information by implementing a table for each prefetch instruction within programs wherein column 606 represents a usage prediction as to whether the data to be prefetched as a result of executing a prefetch instruction will be used or not (*paragraph 0028).*

Refer to claim 1 for motivational statement.

Coulson and Wang et al. does not explicitly teach the apparatus for an identification module configured to associate an identifier with the prefetched data packet prior to receiving the request if prefetched data packet contains the uncorrectable error.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag *(fig. 4, 308)* wherein indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error *(col. 9 lines 15-18).*

Refer to claim 1 for motivational statement.

Coulson, Wang et al. and Rahman et al. does not explicitly teach storing the identifier in the second location with the data packet.

Sharma et al. teach of a CRC encoding scheme for conveying status information by implementing a sending node buffer comprising of an error status bit *(fig. 5, 228, col. 7 lines 24-43).*

Refer to claim 1 for motivational statement.

In regard to claim 8, Coulson disclosed the apparatus of claim 6, wherein the data transfer interface is configured to signal an interrupt to initiate the error recovery process in response to the identifier *(a doorbell/interrupt when a command is to be executed, col. 7 lines 23-28).*

In regard to claim 9, Coulson disclosed the apparatus of claim 6, wherein the identifier is stored in the second location with the prefetched data packet *(command block is constructed in*

command structure cache and stored in main memory to be transfer to sector buffer on a read/write operation, fig. 2, 221, 202-1, 213, col. 7 lines 10-22 and col. 6 lines 41-51 and lines 62-66).

In regard to claim 10, Coulson disclosed the apparatus of claim 6, wherein the data transfer interface is further configured to store an address of the prefetched data packet within the first location (*command block stored in main memory contains an address in mass storage portion and address in main memory portion, fig. 2, 202-1, 202-2, col. 7 lines 14-22).*

In regard to claim 11, Coulson disclosed a system for managing errors in prefetched data, comprising:

a memory interface module configured to prefetch a data packet from a memory array (*main memory, fig. 2, 202-1, col. 6 lines 41-51)* to a temporary buffer (*memory interface, fig. 2, 203, col. 3 lines 24-31)*;

a validation module in communication with the memory interface module, the validation module configured to determine whether the prefetched data packet contains an uncorrectable error (*ECC correction circuitry, fig. 2, 207, col. 3 lines 1-4)*;

a communication module in communication with the temporary buffer, the communication module configured to transmit the prefetched data from the temporary buffer across a communication bus to a requesting device (*memory interface contains sector buffer which transfer requested data to the processor after the error correction has check and correct data, fig. 3, 213, col. 6 lines 41-51)* if the request is received ; and

an error recovery module in communication with the communication module (*Control unit, fig. 2, 206, col. 2 lines 66-67 and col. 3 lines 1-4)*, the error recovery module configured to selectively initiate an error recovery process for the prefetched data packet (*ECC correction circuitry, fig. 2, 207, col. 3 lines 24-31, it is inherent that the ECC correction circuitry contains check bits that is compared to other previously stored check bits to determines for an error if there are variations (Dixon et al. US 6,223,309 col. 6 lines 37-40)* and the prefetched data packet has been transmitted by the communication module (*ECC correction circuitry, fig. 2, 207, col. 3 lines 24-31).*

Coulson does not explicitly teach the apparatus for managing errors in prefetched data by aniticipation of receiving a request for the prefetched data packet prior to receiving the request.

Wang et al. teach the method and apparatus for dynamically conditioning statically produced load speculation and prefetches using runtime information by implementing a table for each prefetch instruction within programs wherein column 606 represents a usage prediction as to whether the data to be prefetched as a result of executing a prefetch instruction will be used or not (*paragraph 0028).*

Refer to claim 1 for motivational statement.

Coulson and Wang et al. does not explicitly teach the apparatus for an identification module configured to associate an identifier with the prefetched data packet prior to receiving the request if prefetched data packet contains the uncorrectable error.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag (*fig. 4, 308)* wherein

indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error (*col. 9 lines 15-18).*

Refer to claim 1 for motivational statement.

Coulson, Wang et al. and Rahman et al. does not explicitly teach storing the identifier in the temporary buffer with the data packet.

Sharma et al. teach of a CRC encoding scheme for conveying status information by implementing a sending node buffer comprising of an error status bit (*fig. 5, 228, col. 7 lines 24-43).*

Refer to claim 1 for motivational statement.

In regard to claim 13, Coulson disclosed the system of claim 11, wherein the identifier is stored in the temporary buffer with the prefetched data packet that contains an uncorrectable error (*sector buffer, fig. 3, 213, col. 6 lines 41-51).*

In regard to claim 14, Coulson disclosed the system of claim 11, wherein the validation module is further configured to store an address that contains an uncorrectable error within the memory array of the prefetched data (*command block stored in main memory contains an address in mass storage portion and address in main memory portion, fig. 2, 202-1, 202-2, col. 7 lines 14-22).*

It is inherent that the ECC correction circuitry contains check bits that are compared to previously check bits stored in system memory to determined an error if there are variations

(Dixon et al. US 6,223,309 col. 6 lines 37-40).

In regard to claim 15, Coulson disclosed the system of claim 11, wherein the error recovery module is further configured to set a flag in response to transmission of prefetched data that contains an uncorrectable error, and wherein the validation module is configured to signal an interrupt to initiate an error recovery process in response to the flag (*a doorbell/interrupt when a command is to be executed, col. 7 lines 23-28).*

In regard to claim 16, Coulson disclosed a method for managing errors in prefetched data, the method comprising:

prefetching a data packet (*read entire sector of main memory into sector buffer, col. 6 lines 62-67)* from a first location (*main memory, fig. 2, 202-1, col. 6 lines 41-51)* into a second location (*sector buffer, fig. 3, 213, col. 6 lines 41-51)*;

determining that the prefetched data packet contains at least one uncorrectable error (*error correction code is used to check transfer to error correction unit if there is an error, fig. 2, 207, col. 6 lines 41-67)*;

determining that the prefetched data packet in the second location has been transmitted for an intended use (*high speed mass storage device to perform main memory and mass storage functions, col. 2 lines 29-32)* in response to the request; and

selectively (*examiner interpret the selective process as first come first server in regard to the ECC error correction)* initiating an error recovery process (*ECC checking/correction circuitry, fig. 2, 207, col. 3 lines 1-4)* only for the prefetched data packet (*ECC correction*

circuitry, fig. 2, 207, col. 3 lines 24-31, It is inherent that the ECC correction circuitry contains check bits that is compared to other previously stored check bits to determines for an error if there are variations (Dixon et al. US 6,223,309 col. 6 lines 37-40) and the prefetched data packet has been transmitted for an intended use (*high speed mass storage device to perform main memory and mass storage functions, col. 2 lines 29-32).*

Coulson does not explicitly teach the apparatus for managing errors in prefetched data by aniticipation of receiving a request for the prefetched data packet prior to receiving the request.

Wang et al. teach the method and apparatus for dynamically conditioning statically produced load speculation and prefetches using runtime information by implementing a table for each prefetch instruction within programs wherein column 606 represents a usage prediction as to whether the data to be prefetched as a result of executing a prefetch instruction will be used or not (*paragraph 0028).*

Refer to claim 1 for motivational statement.

Coulson and Wang et al. does not explicitly teach the apparatus for an identification module configured to associate an identifier with the prefetched data packet prior to receiving the request if prefetched data packet contains the uncorrectable error.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag (*fig. 4, 308)* wherein indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error (*col. 9 lines 15-18).*

Refer to claim 1 for motivational statement.

Coulson, Wang et al. and Rahman et al. does not explicitly teach storing the identifier in the second location with the data packet.

Sharma et al. teach of a CRC encoding scheme for conveying status information by implementing a sending node buffer comprising of an error status bit (*fig. 5, 228, col. 7 lines 24-43).*

Refer to claim 1 for motivational statement.

In regard to claim 18, Coulson disclosed the method of claim 16, further comprising signaling an interrupt to initiate the error recovery process in response to the identifier for the prefetched data packet (*a doorbell/interrupt when a command is to be executed, col. 7 lines 23-28).*

In regard to claim 19, Coulson disclosed the method of claim 16, further comprising storing the identifier in the second location with the prefetched data packet (*command block is constructed in command structure cache and stored in main memory to be transfer to sector buffer on a read/write operation, fig. 2, 221, 202-1, 213, col. 7 lines 10-22 and col. 6 lines 41-51 and lines 62-66).*

In regard to claim 20, Coulson disclosed the method of claim 16, further comprising storing an address for the prefetched data packet within the first location (*command block stored in main memory contains an address in mass storage portion and address in main memory*

portion, fig. 2, 202-1, 202-2, col. 7 lines 14-22).

In regard to claim 22, Coulson disclosed an apparatus for managing errors in prefetched data, comprising:

means (*control unit, fig. 2, 206, col. 3 lines 24-31)* for prefetching a data packet (*read entire sector of main memory into sector buffer, col. 6 lines 62-67)* from a first location (*main memory, fig. 2, 202-1, col. 6 lines 41-51)* into a second location (*sector buffer, fig. 3, 213, col. 6 lines 41-51)*;

means for determining that the prefetched data packet contains at least one uncorrectable error (*error correction code is used to check transfer to error correction unit if there is an error, fig. 2, 207, col. 6 lines 41-67)*;

means for determining that the prefetched data packet in the second location has been transmitted for an intended use (*high speed mass storage device to perform main memory and mass storage functions, col. 2 lines 29-32)* in response to the request; and

means for selectively (*examiner interpret the selective process as first come first server in regard to the ECC error correction)* initiating an error recovery process (*ECC checking/correction circuitry, fig. 2, 207, col. 3 lines 1-4)* only for the prefetched data packet (*ECC correction circuitry, fig. 2, 207, col. 3 lines 24-31, it is inherent that the ECC correction circuitry contains check bits that is compared to other previously stored check bits to determines for an error if there are variations (Dixon et al. US 6,223,309 col. 6 lines 37-40)* and the prefetched data packet has been transmitted for an intended use (*high speed mass storage device to perform main memory and mass storage functions, col. 2 lines 29-32).*

Coulson does not explicitly teach the apparatus for managing errors in prefetched data by aniticipation of receiving a request for the prefetched data packet prior to receiving the request.

Wang et al. teach the method and apparatus for dynamically conditioning statically produced load speculation and prefetches using runtime information by implementing a table for each prefetch instruction within programs wherein column 606 represents a usage prediction as to whether the data to be prefetched as a result of executing a prefetch instruction will be used or not (*paragraph 0028).*

Refer to claim 1 for motivational statement.

Coulson and Wang et al. does not explicitly teach the apparatus for an identification module configured to associate an identifier with the prefetched data packet prior to receiving the request if prefetched data packet contains the uncorrectable error.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag (*fig. 4, 308)* wherein indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error (*col. 9 lines 15-18).*

Refer to claim 1 for motivational statement.

Coulson, Wang et al. and Rahman et al. does not explicitly teach storing the identifier in the second location with the data packet.

Sharma et al. teach of a CRC encoding scheme for conveying status information by implementing a sending node buffer comprising of an error status bit (*fig. 5, 228, col. 7 lines 24-43).*

Refer to claim 1 for motivational statement.

In regard to claim 24, Coulson disclosed the apparatus of claim 22, further comprising means for signaling an interrupt to initiate the error recovery process in response to the identifier for the prefetched data packet (*a doorbell/interrupt when a command is to be executed, col. 7 lines 23-28).*

In regard to claim 25, Coulson disclosed the apparatus of claim 22, further comprising means for storing the identifier in the second location with the prefetched data packet (*command block is constructed in command structure cache and stored in main memory to be transfer to sector buffer on a read/write operation, fig. 2, 221, 202-1, 213, col. 7 lines 10-22 and col. 6 lines 41-51 and lines 62-66).*

In regard to claim 26, Coulson disclosed the apparatus of claim 22, further comprising means for storing an address within the first location for the prefetched data packet (*command block stored in main memory contains an address in mass storage portion and address in main memory portion, fig. 2, 202-1, 202-2, col. 7 lines 14-22).*

In regard to claim 27, Coulson disclosed an article of manufacture comprising a program storage medium readable by a processor and embodying one or more instructions executable by a processor to perform a method for managing errors in prefetched data, the method comprising:

prefetching data packet (*read entire sector of main memory into sector buffer, col. 6 lines 62-67)* from a first location (*main memory, fig. 2, 202-1, col. 6 lines 41-51)* into a second location (*sector buffer, fig. 3, 213, col. 6 lines 41-51)*;

determining that the prefetched data packet contains at least one uncorrectable error (*error correction code is used to check transfer to error correction unit if there is an error, fig. 2, 207, col. 6 lines 41-67)*;

determining that the prefetched data packet in the second location has been transmitted for an intended use (*high speed mass storage device to perform main memory and mass storage functions, col. 2 lines 29-32)* in respone to the request; and

selectively (*examiner interpret the selective process as first come first server in regard to the ECC error correction)* initiating an error recovery process (*ECC checking/correction circuitry, fig. 2, 207, col. 3 lines 1-4)* for the prefetched data packet (*ECC correction circuitry, fig. 2, 207, col. 3 lines 24-31, it is inherent that the ECC correction circuitry contains check bits that is compared to other previously stored check bits to determines for an error if there are variations (Dixon et al. US 6,223,309 col. 6 lines 37-40)* and the prefetched data packet has been transmitted for an intended use (*high speed mass storage device to perform main memory and mass storage functions, col. 2 lines 29-32).*

Coulson does not explicitly teach the apparatus for managing errors in prefetched data by aniticipation of receiving a request for the prefetched data packet prior to receiving the request.

Wang et al. teach the method and apparatus for dynamically conditioning statically produced load speculation and prefetches using runtime information by

implementing a table for each prefetch instruction within programs wherein column 606 represents a usage prediction as to whether the data to be prefetched as a result of executing a prefetch instruction will be used or not *(paragraph 0028)*.

Refer to claim 1 for motivational statement.

Coulson and Wang et al. does not explicitly teach the apparatus for an identification module configured to associate an identifier with the prefetched data packet prior to receiving the request if prefetched data packet contains the uncorrectable error.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag *(fig. 4, 308)* wherein indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error *(col. 9 lines 15-18)*.

Refer to claim 1 for motivational statement.

Coulson, Wang et al. and Rahman et al. does not explicitly teach storing the identifier in the second location with the data packet.

Sharma et al. teach of a CRC encoding scheme for conveying status information by implementing a sending node buffer comprising of an error status bit *(fig. 5, 228, col. 7 lines 24-43)*.

Refer to claim 1 for motivational statement.

In regard to claim 29, Coulson disclosed the article of manufacture of claim 27, wherein the method further comprises signaling an interrupt to initiate the error recovery process in response to the identifier for the prefetched data packet *(a doorbell/interrupt when a command is*

to be executed, col. 7 lines 23-28).

In regard to claim 30, Coulson disclosed the article of manufacture of claim 29, the method further comprising storing an address for the prefetched data packet within the first location (*command block stored in main memory contains an address in mass storage portion and address in main memory portion, fig. 2, 202-1, 202-2, col. 7 lines 14-22).*

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5. Claims 5 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson (US 6,345,349) in further view of Wang et al. (US 2004/0117606) in further view of Rahman et al. (US 5,590,337) in further view of Sharma et al. (US 7,047,475) in further view of Imazato (US 6,678,858).

In regard to claim 5, Coulson and Wang et al. does not teaches the apparatus of claim 1, wherein the error recovery module is configured to set a flag in response to transfer of the prefetched data packet, and wherein the validation module is configured to signal an interrupt to initiate the error recovery process in response to the set flag.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag (*fig. 4, 308)* wherein indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error (*col. 9 lines 15-18).*

Refer to claim 1 for motivational statement.

Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the configuration of signaling an interrupt to initiate the error recovery process.

Imazato disclosed the code error monitoring apparatus where the EACK_B is a flag signal to acknowledge a detection of code error (*col. 11 lines 7-13)* and the INT_B interrupt the process executed in the CPU (*col. 11 lines 28-30).*

It would have been obvious to modify the apparatus of Coulson, Wang et al., Rahman et al. and Sharma et al. by adding Imazato code error monitoring apparatus. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would prevent malfunction due to a code error and improve reliability and quality (*col. 4 lines 26-31).*

In regard to claim 21, Coulson and Wang et al. does not teaches the method of claim 16, further comprising: setting a flag in response to transmission of the prefetched data packet; and interrupting a data transfer of prefetched data in response to the flag.

Rahman et al. teach the processor interface chip for dual-microprocessor processor system implementing an uncorrectable memory error flag (*fig. 4, 308)* wherein indication is not passed on to the microprocessor until the microprocessor actually requests the data, which causes the error (*col. 9 lines 15-18).*

Refer to claim 1 for motivational statement.

Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the configuration of signaling an interrupt to initiate the error recovery process.

Imazato disclosed the code error monitoring apparatus where the EACK_B is a flag signal to acknowledge a detection of code error *(col. 11 lines 7-13)* and the INT_B interrupt the process executed in the CPU *(col. 11 lines 28-30).*

Refer to claim 5 for motivational statement.

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6. Claims 31-36 are rejected under 35 U.S.C 103(a) as being unpatentable over Coulson (US 6,345,349) in further view of Wang et al. (US 2004/0117606) in further view of Rahman et al. (US 5,590,337) in further view of Sharma et al. (US 7,047,475) in further view of Shin et al. (US 2002/0157054).

In regard to claim 31, Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the apparatus of claim 1, wherein the error recovery process comprises re-retrieving the data packet from the first location.

Shin et al. teach the system for host handling of communication errors by the initiating host retransmit the request to retrieve the data from the data store device in handling of error *(paragraph 0124).*

It would have been obvious to modify the apparatus of Coulson and Wang et al., Rahman et al. and Sharma et al. by adding Shin et al. system for host handling of communication errors. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would increase the speed of communication between hosts and data store devices *(paragraph 0003).*

In regard to claim 32, Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the apparatus of claim 6, wherein the error recovery process comprises re-retrieving the data packet from the first location.

Shin et al. teach the system for host handling of communication errors by the initiating host retransmit the request to retrieve the data from the data store device in handling of error (*paragraph 0124).*

Refer to claim 31 for motivational statement.

In regard to claim 33, Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the apparatus of claim 11, wherein the error recovery process comprises re-retrieving the data packet from the memory array.

Shin et al. teach the system for host handling of communication errors by the initiating host retransmit the request to retrieve the data from the data store device in handling of error (*paragraph 0124).*

Refer to claim 31 for motivational statement.

In regard to claim 34, Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the method of claim 16, wherein the error recovery process comprises re-retrieving the data packet from the first location.

Shin et al. teach the system for host handling of communication errors by the initiating host retransmit the request to retrieve the data from the data store device in handling of error (*paragraph 0124).*

Refer to claim 31 for motivational statement.

In regard to claim 35, Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the apparatus of claim 22, wherein the error recovery process comprises re-retrieving the data packet from the first location.

Shin et al. teach the system for host handling of communication errors by the initiating host retransmit the request to retrieve the data from the data store device in handling of error (*paragraph 0124).*

Refer to claim 31 for motivational statement.

In regard to claim 36, Coulson, Wang et al., Rahman et al. and Sharma et al. does not teach the article of manufacture of claim 27, wherein the error recovery process comprises re-retrieving the data packet from the first location.

Shin et al. teach the system for host handling of communication errors by the initiating host retransmit the request to retrieve the data from the data store device in handling of error (*paragraph 0124).*

Refer to claim 31 for motivational statement.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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